REMARKS

Applicant respectfully requests reconsideration of the subject application as in light of the amendments and remarks. Claims 1, 11, 19, 20, 25, 32, 38, and 52 have been amended and claim 27 has been canceled. The amendments to the claims have been made in an effort to expedite the prosecution of this matter, without limiting the scope of the invention and only in an effort to impart precision to the claims (e.g., by more particularly pointing out the invention, rather than to avoid prior art). As a result, claims 1-26, 28-35, 38-40, 52, and 53 are now pending. No new matter is believed to have been introduced hereby.

Claim 20 was objected to under 37 C.F.R. §1.75 for being of improper dependent form. In response, claim 20 has been amended as detailed above to recite other language and is now believed to be in proper dependent form.

Claims 1, 2, 4-8, 10, 11, 12, 14-18, 25-26, 28, 29, and 31 stand rejected under 35 U.S.C. §102(b) as being anticipated by "Optimizing the DRAM Refresh Count for Merged DRAM/Logic LSIs" by Ohsawa et al. (hereinafter "Ohsawa"). Claims 1-5, 7, 8, 10-16, 18-20, 23-27, 29, 31-33, 35, 38-39, 52, and 53 stand rejected under 35 U.S.C. §102(e) over Boyer et al. (hereinafter "Boyer"). Claims 6, 9, 17, 21, 22, 28, 30, 34, and 40 stand rejected under 35 U.S.C. §103(a) over Boyer in view of Ohsawa. Claims 3, 9, 13, 19, 21-24, 27, 30, 32-35, 38-40, 52, and 53 stand rejected under 35 U.S.C. §103(a) over Ohsawa in view of Boyer.

Claims 1-10

Claim 1 as amended in part recites that "the use registers are implemented adjacent to the memory cells." It is respectfully submitted that none of the cited references alone, or in combination, teach, disclose, or suggest the claimed combination of the features such as set forth in claim 1.

First, with respect to Boyer, the Office Action fails to identify any "use registers" at all in rejecting claim 1. In particular, the section 102(e) rejection merely states that "Boyer discloses a method and apparatus for leveraging history bits to optimize memory refresh performance." [Emphasis Added.] Next, the Office Action points to numerous sections within the Boyer patent without identifying any specific recitations of any rejected claims.

The undersigned respectfully submits that after reviewing the identified sections he is unsure as to how these sections relate to the claimed combination of features such as set forth in claim 1. However, in an effort to expedite the prosecution of this matter, claim 1 has been amended as detailed above, without limiting the scope of the invention and only in an effort to impart precision to the claims (e.g., by more particularly pointing out the invention, rather than to avoid prior art).

If there is to be another Office Action issued rejecting the claims under section 102, it is hereby respectfully requested that specifics regarding rejection of each claim be made on the record, so that the applicant may appropriately respond

to the rejections. In any case, Boyer at a minimum fails to teach, disclose, or suggest any "use registers" or that the use registers being "implemented adjacent to the memory cells" (see, e.g., Fig. 2 of Boyer). Accordingly, claim 1 is patentable over the section 102(e) rejection based on Boyer.

Second, with respect to Ohsawa, the outstanding Office Action states that "Ohsawa shows these memory cells and use registers together in a single 'memory unit' in Fig. 4" (page 9, fourth paragraph). In response, it is respectfully submitted that Fig. 4 of Ohsawa fails to anticipate the claimed combination of features such as set fourth in claim 1.

In particular, section 3.1 of Ohsawa (which discusses Figs. 4 and 5) indicates that the refresh flags are provided by the "DRAM controller" and not "adjacent to the memory cells" such as claimed in the amended claim 1 (see, section 3.1, first sentence of third paragraph). Ohsawa also clearly intends Fig. 4 to be a mere illustration of "correspondence" between the refresh flag and each corresponding row, rather than a design criterion (where Ohsawa states in the second sentence of the third paragraph of section 3.1 that each "row is refreshed when the corresponding refresh flag is 1 (see Fig. 4)" [emphasis added]). In fact, the fourth paragraph of section 3.1 states that Fig. 5 "shows the SRA architecture in detail" [emphasis added]. This fact is evident as the Office Action also indicates that "Fig. 5 is not explicitly labeled 'memory unit.'"

The undersigned appreciates the Examiner's statements that it "is not clear why Ohsawa mentions DRAM controller since he doesn't show it in the figures" or that a typical interpretation "doesn't seem to match Ohsawa's disclosure and figures." It is respectfully submitted that "perhaps" the Examiner is affording this "poor translation from Japanese" more credit than it really deserves. The only explanation for these discrepancies is that Ohsawa clearly intended Fig. 4 not to be anything more than a simplification of Fig. 5 (i.e., showing correspondence between the refresh flag and each row as discussed above). Accordingly, it is respectfully submitted that reading Ohsawa any broader runs afoul the requirements of U.S. law (e.g., 35 U.S.C. §§102 and 103). And, claim 1 is clearly patentable over the cited references and is in condition for allowance.

Claims 2-9 are dependent claims and should be allowable by virtue of their dependency on respective base claim 1, as well as for the additional recitations they contain.

Furthermore, with respect to claim 2, it is respectfully submitted that the claimed self-refresh logic is not taught, disclosed, or suggested by the cited art, alone or in combination. In particular, the outstanding Office Action states that Ohsawa's static mode is a self-refresh mode, citing that the entire disclosure is directed toward reducing the power consumed and that the applicant has failed to present any evidence whatsoever that Ohsawa's static or standby modes are different than the claimed self-refresh logic.

In response, it is cordially submitted that Ohsawa does not contemplate a self-refresh logic on a memory device at all. For example, the discussion of items (1) and (2) at the end of section 3.1 are evidence of Ohsawa's ignorance regarding this feature (and the claimed combination of features). More specifically, paragraph 5 of section 3.1 states that Ohsawa's approach (SRA) has difficulty stopping a refresh. This is in part because Ohsawa only envisions using a DRAM controller for providing its refresh flag (as discussed in more detail above). Accordingly, Ohsawa's SRA approach is internally inconsistent with the claimed "self-refresh logic on the memory device", for example where the use registers are implemented "adjacent to the memory cells." Accordingly, claim 2 is in condition for allowance.

Claims 11-18

Claim 11 as amended in part recites that "the use registers are implemented adjacent to the memory cells." It is respectfully submitted that none of the cited references alone, or in combination, teach, disclose, or suggest the claimed combination of the features such as set forth in claim 11 (see, e.g., the discussion of claim 1 above). Accordingly, claim 11 is in condition for allowance at least for similar reasons as claim 1.

Claims 12-18 are dependent claims and should be allowable by virtue of their dependency on respective base claim 11, as well as for the additional limitations they contain. For example, claim 12 is also allowable in part because of similar reasons as discussed with respect to claim 2 above.

Claims 19-24

Claim 19 as amended in part recites "the use registers" and "refresh logic on one of the memory devices." It is respectfully submitted that none of the cited references alone, or in combination, teach, disclose, or suggest the claimed combination of the features such as set forth in claim 19 (see, e.g., the discussion of claims 1 and 2 above). Accordingly, claim 19 is in condition for allowance at least for respectively similar reasons as claims 1 and 2.

Claims 20-24 are dependent claims and should be allowable by virtue of their dependency on respective base claim 19, as well as for the additional limitations they contain.

Claims 25-26 and 28-31

Claim 25 as amended in part recites "recent-access flags associated with the memory and implemented adjacent to the memory cells." It is respectfully submitted that none of the cited references alone, or in combination, teach, disclose, or suggest the claimed combination of the features such as set forth in claim 25. For example, as discussed above with reference to claim 1, none of the cited references, alone or in combination, teach, disclose, or suggest the "use registers implemented adjacent to the memory cells." Similarly, these references fail to anticipate the claimed "recent-access flags associated with the memory and implemented adjacent to the memory cells" or otherwise the claimed combination

of features such as set forth in the amended claim 25. Accordingly, claim 25 is in condition for allowance.

Claims 26 and 28-31 are dependent claims and should be allowable by virtue of their dependency on respective base claim 25, as well as for the additional limitations they contain.

Claims 32-35

Claim 32 as amended in part recites that "the determining act is performed by utilizing a plurality of recent-access flags associated with each of the memory rows and implemented adjacent to the memory rows." [Emphasis Added.] It is respectfully submitted that none of the cited references alone, or in combination, teach, disclose, or suggest the claimed combination of the features such as set forth in claim 32. For example, similarly to the discussion with reference to claim 25, none of the cited references, alone or in combination, teach, disclose, or suggest the claimed "recent-access flags associated with each of the memory rows and implemented adjacent to the memory rows" or otherwise the claimed combination of features such as set forth in the amended claim 32. Accordingly, claim 32 is in condition for allowance.

Claims 33-35 are dependent claims and should be allowable by virtue of their dependency on respective base claim 32, as well as for the additional limitations they contain.

Claims 38-40

Claim 38 as amended in part recites that "the keeping track action is performed by utilizing a plurality of recent-access flags that are implemented adjacent to the memory cells." [Emphasis Added.] It is respectfully submitted that none of the cited references alone, or in combination, teach, disclose, or suggest the claimed combination of the features such as set forth in claim 38. For example, as discussed above with reference to claim 25, none of the cited references, alone or in combination, teach, disclose, or suggest the claimed "recent-access flags" that are "implemented adjacent to the memory cells" or otherwise the claimed combination of features such as set forth in the amended claim 38. Accordingly, claim 38 is in condition for allowance.

Claims 39 and 40 are dependent claims and should be allowable by virtue of their dependency on respective base claim 38, as well as for the additional limitations they contain.

Claims 52 and 53

Claim 52 as amended in part recites that "the keeping track action is performed by utilizing a plurality of recent-access flags that are implemented adjacent to the memory cells." [Emphasis Added.] It is respectfully submitted that none of the cited references alone, or in combination, teach, disclose, or suggest the claimed combination of the features such as set forth in claim 52 (e.g., as discussed above with respect to claim 38). Accordingly, claim 52 is in condition for allowance.

Claim 53 is a dependent claim and should be allowable by virtue of its dependency on respective base claim 52, as well as for the additional limitations they contain.

CONCLUSION

Applicant respectfully submits that claims 1-26, 28-35, 38-40, and 52-53 are in condition for allowance.

Should any matter in this case remain unresolved, the undersigned attorney respectfully requests a telephone conference with the Examiner to resolve any such outstanding matter.

Respectfully Submitted,

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Ramin Aghevli

Ramin Aghevli
Reg. No. 43,462
303.539.0265 x240